

Please ADD the following claims:

14. (NEW) A semiconductor device comprising:

- ✓ <sup>23</sup> a first insulating layer;
- ✓ <sup>22</sup> a first conductive layer having wiring patterns formed under the first insulating layer;
- <sup>24</sup> a second conductive layer having wiring patterns formed over the first insulating layer, one or more of the wiring patterns of the second conductive layer being electrically connected to one or more of the wiring patterns of the first conductive layer through via holes; and
- ✓ <sup>30</sup> at least one semiconductor element imbedded inside the first insulating layer and electrically connected to at least one of the wiring patterns of the first conductive layer and at least one of the wiring patterns of the second conductive layer.

β<sup>2</sup> ✓ 15. (NEW) The semiconductor device according to claim 14, further comprising a second insulating layer having at least one semiconductor element imbedded therein, the second insulating layer being separated from the first insulating layer by one of the first and second conductor layers, and the at least one semiconductor element of the second insulating layer being electrically connected to one or more of the wiring patterns of the first and second conductor layers.

✓ 16. (NEW) The semiconductor device according to claim 14, wherein one or more of the wiring patterns of the first conductor layer are electrically connected to one or more of the wiring patterns of the second conductor layer.

17. (NEW) A semiconductor device comprising:

- ✓ <sup>23</sup> a first insulating layer formed over a <sup>22</sup> first conductor layer, the first insulating layer having at least one <sup>30</sup> semiconductor element imbedded therein and the first conductor layer having wiring patterns therein; and
- ✓ <sup>24</sup> a second insulating layer formed over a <sup>25</sup> second conductor layer, the second insulating layer and conductor layer being formed over the first insulating layer and first conductor layer, the second insulating layer having at least one semiconductor element imbedded therein and